

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

III. Amendments to the Claims.

1. (Currently Amended) A memory controller connected to a semiconductor memory device, comprising:

- 5 a clock generating circuit that generates an output clock signal;  
a data ~~generating~~ storing circuit that provides output digital data;  
a predetermined number "m" data output terminals that provide output data to the semiconductor memory device in parallel;  
m output holding circuits for storing the output digital data synchronously  
10 with the output clock signal;  
a predetermined number "n" signal output terminals that provide output strobe signals to the semiconductor memory device in synchronism with the output data, where  $n < m$ ; and  
a plurality of output delay circuits including one output delay circuit for  
15 every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s);  
a circuit core region in which the clock generating circuit and data ~~generating~~ storing circuit are formed; and  
20 an interface region surrounding the circuit core region in which the data output terminals, output holding circuits, signal output terminals, and output delay circuits are formed; wherein  
each one of the m output holding circuits is adjacent to a corresponding one of the m data output terminals ~~in a first direction~~ and between the  
25 corresponding data output terminal and the circuit core region; and  
an output of each one of the output delay circuits is adjacent to the corresponding p signal output terminal(s) ~~in the first direction~~ and between the corresponding signal output terminal and the circuit core region.

2. (Currently Amended) The memory controller of claim 1, wherein:

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

the m output data output terminals and n signal output terminals are aligned with one another in a ~~second~~ first direction;

the m holding circuits are aligned with one another in the ~~second~~ first direction; and

5 the plurality of output delay circuits are aligned with one another in the ~~second~~ first direction between the m holding circuits and the m data output terminals and n signal output terminals.

3. (Original) The memory controller of claim 1, wherein:

the value p is greater than one, and the value n is a multiple of p.

10 4. (Original) The memory controller of claim 1, wherein:

value of p is selected from the group consisting of one and two.

5. (Original) The memory controller of claim 1, wherein:

the value of p is one.

15 6. (Original) The memory controller of claim 1, wherein:

the value of p is two; and

each of the plurality of output delay circuits has an output terminal arranged equidistant from the corresponding two signal output terminals.

7. (Currently Amended) The memory controller of claim 1, further including:

20 a plurality of data input terminals that receive input data from the semiconductor memory device;

a signal input terminal for every "q" data input terminals, where "q" is an integer greater than 2, each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the  
25 input data;

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

an input delay circuit corresponding to each signal input terminal that delays a received device input clock signal from the semiconductor memory device ~~signal~~ by a predetermined amount to generate an input strobe signal, each input delay circuit signal input terminal ~~in the first direction being~~  
5 between the corresponding signal input terminal and the circuit core region and a circuit output terminal position that is offset in ~~the second a~~ first direction with respect to the corresponding signal input terminal, the first direction being parallel to the q data input terminals; and

an input holding circuit corresponding to each data input terminal,  
10 each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit; wherein the input data is transmitted to the data generating storing circuit through the data input terminals.

8. (Previously Presented) The memory controller of claim 1, further including:

15 a plurality of data input terminals that receive input data from the semiconductor memory device;

a signal input terminal for every "q" data input terminals, where "q" is an integer greater than 2, each signal input terminal receiving a device input clock signal from the semiconductor memory device in synchronism with the  
20 input data;

an input delay circuit corresponding to each signal input terminal that delays a received device input clock signal from the semiconductor memory device by a predetermined amount to generate an input strobe signal, the input delay circuits being arranged between the signal input terminals and positions  
25 where the input delay circuits output the input strobe signals; and

an input holding circuit corresponding to each data input terminal, each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit;

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

a first wiring corresponding to each data input terminal that transmits digital data to a corresponding input holding circuit; and

a second wiring corresponding to each input holding circuit that transmits the input strobe signal from a corresponding input delay circuit to the input holding circuit; wherein

the first and second wiring corresponding to each input holding circuit being equal in length.

9. (Original) The memory controller of claim 1, wherein:

the m data output terminals are also data input terminals that receive input data from the semiconductor memory device in parallel; and

the n signal output terminals are also signal input terminals for receiving device input clock signals from the semiconductor memory device in synchronism with the input data.

10. (Original) The memory controller of claim 1, wherein:

the output holding circuits transmit output digital data synchronously with both a rising edge and a falling edge of the output clock signal.

11. (Currently Amended) The memory controller of claim 1, further including:

a plurality of data input terminals that receive input data from the semiconductor memory device;

a signal input terminal for every "q" data input terminals, where "q" is an integer greater than 2, each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data; and

an input delay circuit corresponding to each signal input terminal that delays a received device input clock ~~signal~~ form from the semiconductor memory device ~~signal~~ by a predetermined amount to generate an input strobe signal, each input delay circuit having a circuit input position that is aligned

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

with the corresponding signal input terminal ~~in the first direction~~ between  
the corresponding signal input terminal and the circuit core region and a  
circuit output position that is offset in ~~the second~~ a first direction with respect  
to the corresponding signal input terminal, the first direction being different  
5 than the aligned position direction of the corresponding signal input  
terminal and circuit input position;

an input holding circuit corresponding to each data input terminal,  
each group of q input holding circuits holding input data in synchronism with  
the input strobe signal from a corresponding input delay circuit; wherein  
10 the input holding circuits transmit input data to the data generating  
storing circuit synchronously with both a rising edge and a falling edge of the  
corresponding input strobe signal.

12. (Original) The memory controller of claim 1, further including:

the semiconductor memory device being coupled to the memory controller  
15 by the m data output terminals and the n signal output terminals.

13. (Previously Presented) The memory controller of claim 1, further including:

each output holding circuit comprising a first latch circuit.

14. (Previously Presented) The memory controller of claim 13, further including:

20 the data output terminals are data input/output (I/O) terminals;

the signal output terminals are signal I/O terminals;

m input holding circuits corresponding to the data I/O terminals  
formed in the interface region, each input holding circuit comprising a second  
latch circuit connected to a corresponding data I/O terminal by a first wiring,  
the input holding circuits holding input data in synchronism with a  
25 corresponding input strobe signal; and

an input delay circuit connected to each signal I/O terminal by a  
second wiring, each input delay circuit delaying a received device input clock

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

from the semiconductor memory device signal by a predetermined amount to generate an input strobe signal, each input strobe signal being connected to a corresponding second latch circuit by a third wiring; wherein

the length of the first wiring to each second latch circuit is equal to the sum of the lengths of the second and third wirings corresponding to the same second latch circuit.

15  
**15. (Previously Presented)** A memory controller connected to a semiconductor memory device, comprising:

a predetermined number "m" data input terminals that receive input data from the semiconductor memory device;

a predetermined number "n" signal input terminals, each signal input terminal receiving a device input clock signal from the semiconductor memory device in synchronism with the input data, where  $m > n$ ;

15 a data storing circuit for receiving digital data from the data input terminals;

n input delay circuits that delay received device input clock signals from the semiconductor memory device by a predetermined amount to generate input strobe signals;

20 m input holding circuits that hold the input data in synchronism with the input strobe signals generated by the input delay circuits; and

m data input wirings, each data input wiring transmitting an input data value from one data input terminal to a corresponding input holding circuit; and

25 m signal input wirings transmitting one input strobe signal from one input delay circuit to a corresponding input holding circuit; wherein

the data input wiring and signal input wiring for the same corresponding input holding circuit being equal in length.

16. (Original) The memory controller of claim 15, wherein:

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

the input delay circuits are arranged between the signal input terminals and locations where the input delay circuits output the input strobe signals.

17. (Currently Amended) The memory controller of claim 15, wherein:

the input holding circuits transmit input data to the data **generating**  
5 **storing** circuit synchronously with both a rising edge and a falling edge of the corresponding input strobe signal.

18. (Original) The memory controller of claim 15, further including:

the semiconductor memory device being coupled to the memory controller by the m data input terminals and the n signal input terminals.

10 19. (Original) The memory controller of claim 15, further including:

a circuit core region in which the data storing circuit are formed; and  
an interface region surrounding the circuit core region in which the data  
input terminals, input holding circuits, signal input terminals, input delay circuits,  
signal input wirings, and data input wirings are formed; wherein  
15 each input holding circuit comprising a first latch circuit.

20. (Previously presented) The memory controller of claim 15, further including:

the m data input terminals and n signal input terminals are aligned with  
one another in a first direction; and  
20 the m input holding circuits are aligned with one another in the first  
direction parallel to the data input terminals and signal input terminals.

21. (Currently Amended) The memory controller of claim 15, further including:

a clock generating circuit that generates an output clock signal;  
25 a **the** data **generating storing** circuit **that** provides output **digital** data;  
a plurality of data output terminals **that** that provide **the** output data to the  
semiconductor memory device in parallel;

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

a signal output terminal for every "q" data output terminals, where "q" is an integer greater than 2, each signal output terminal providing an output strobe signal to the semiconductor memory device in synchronism with the output data;

5 an output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s); and

10 an output holding circuit corresponding to each data output terminal, each group of q output holding circuits holding output data in synchronism with the output strobe signal from the corresponding output delay circuit.